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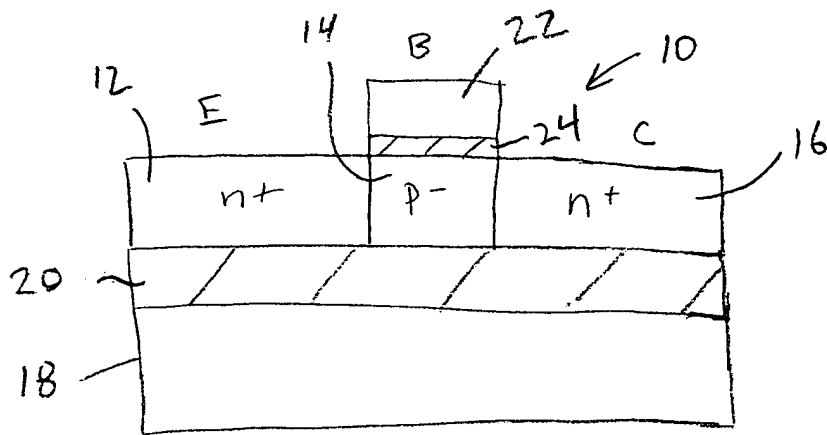


FIG. 1
- PRIOR ART -

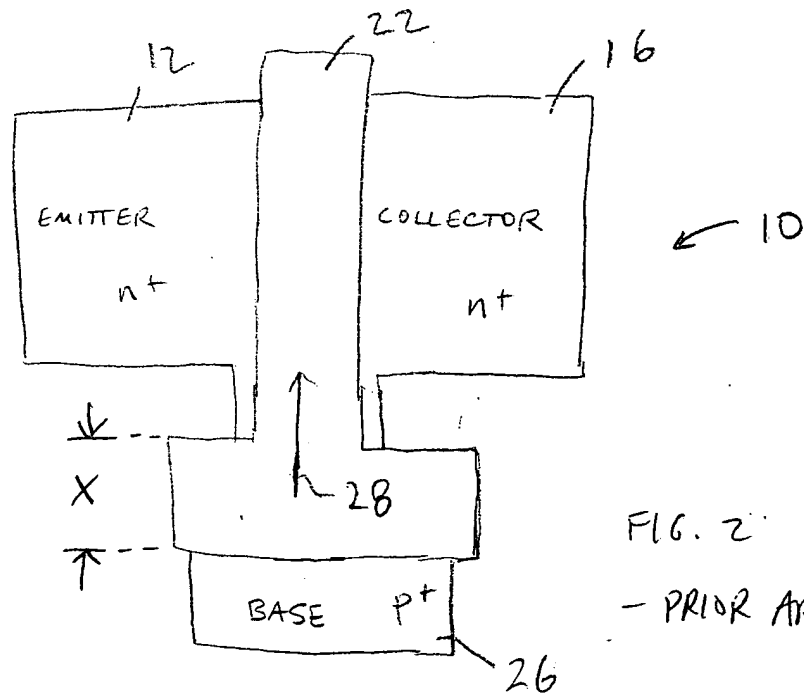


FIG. 2
- PRIOR ART -

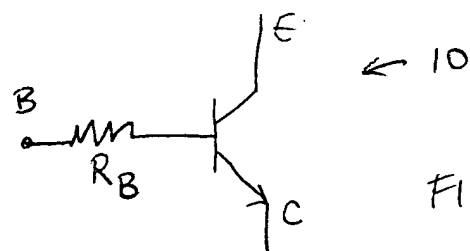


FIG. 3
- PRIOR ART -

Hand-drawn schematic of a 128-bit memory array. The array is divided into four sections labeled E, B, C, and S. Section E contains a p+ block and an n+ block. Section B contains a p- block and an n+ block. Section C contains an n+ block and a p- block. Section S contains a p- block and an n+ block. The array is labeled with 'E', 'B', 'C', and 'S' above the top row, and 'p+', 'p-', 'n+', 'n+', 'p-', 'n+' below the top row. The array is labeled with '60' and '64' on the left side, indicating the number of bits in each row.

FIG. 5

30

32

1 2 1

66

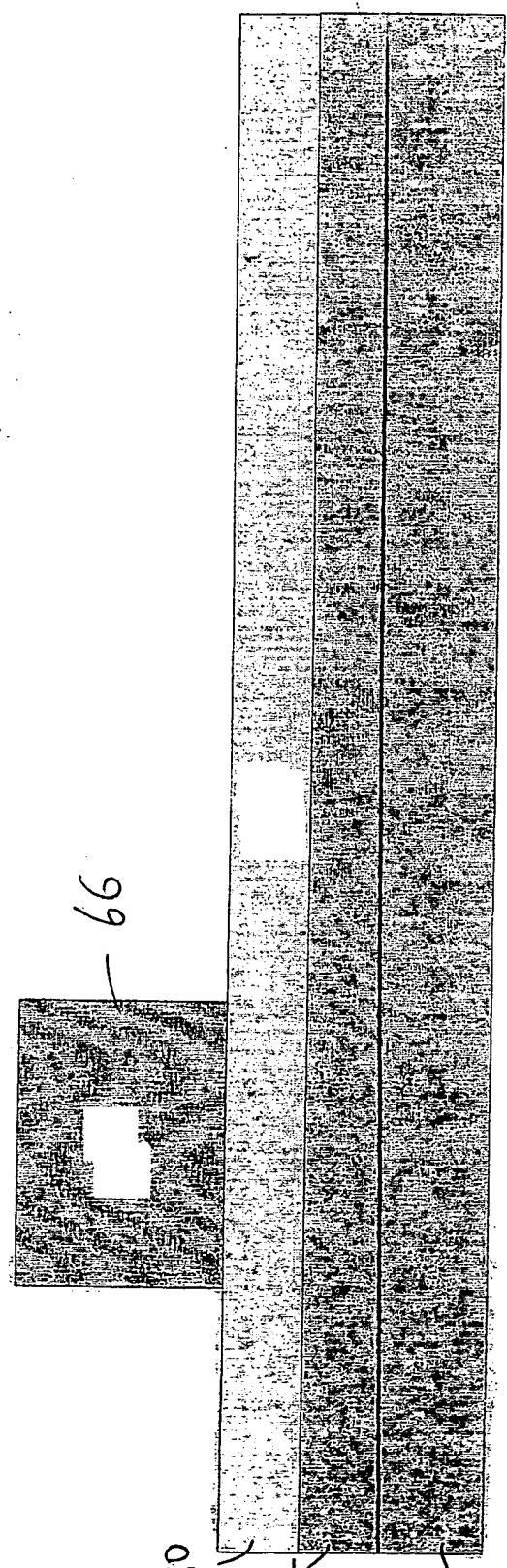
60

58

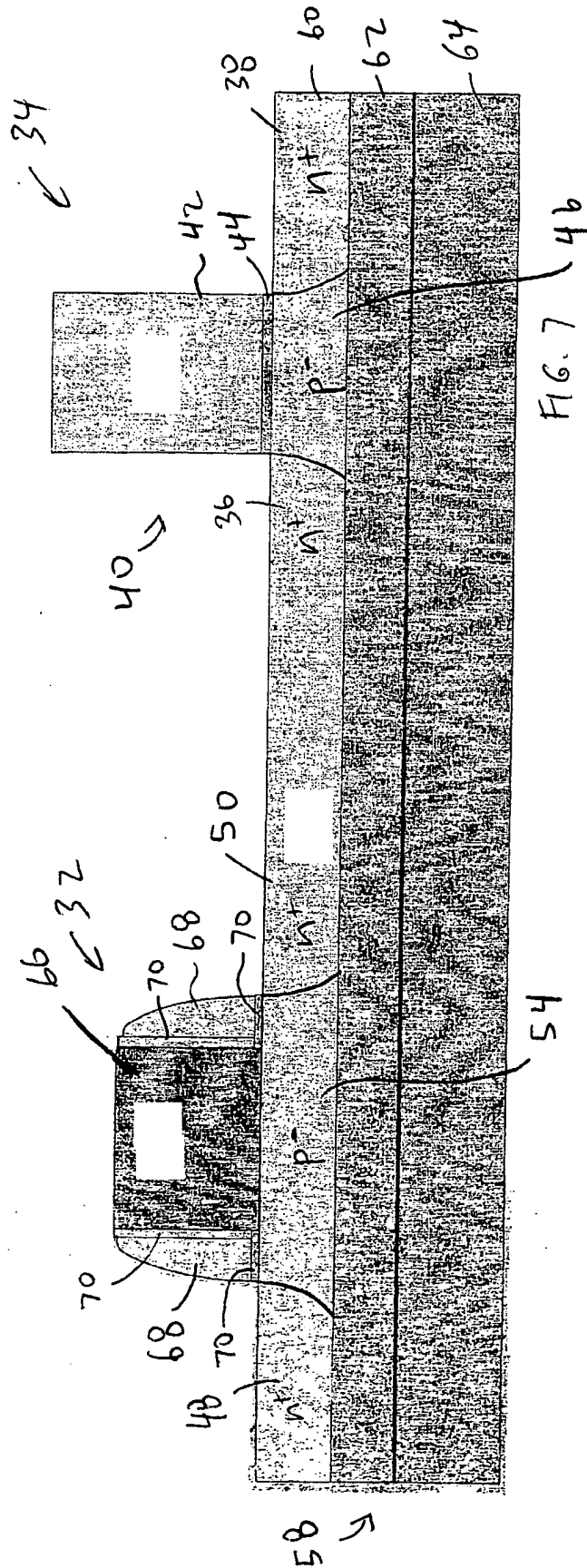
62

64

FIG. 6



30



30

32

34

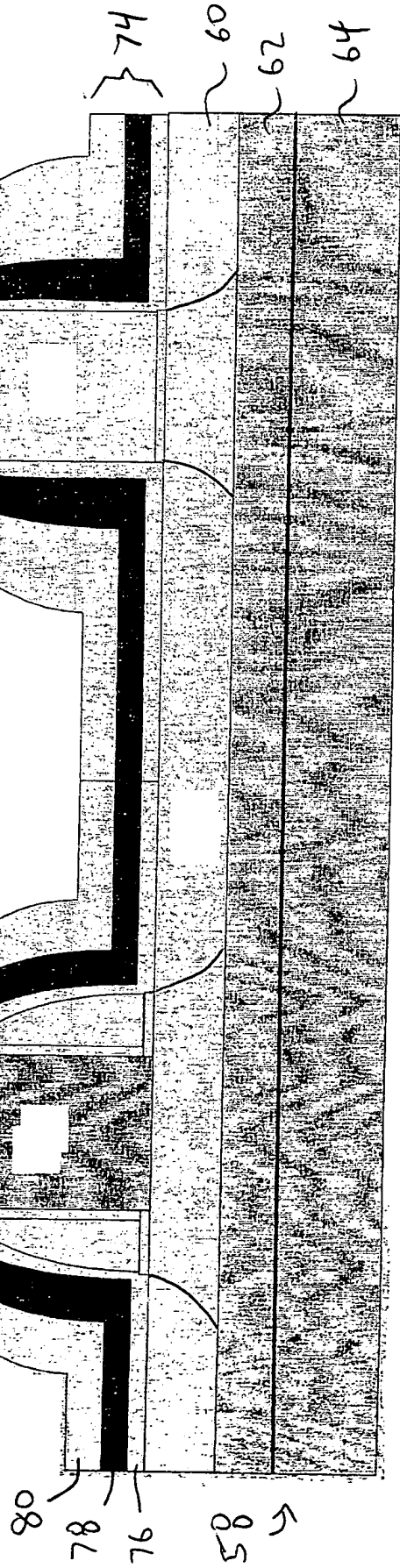


FIG. 8

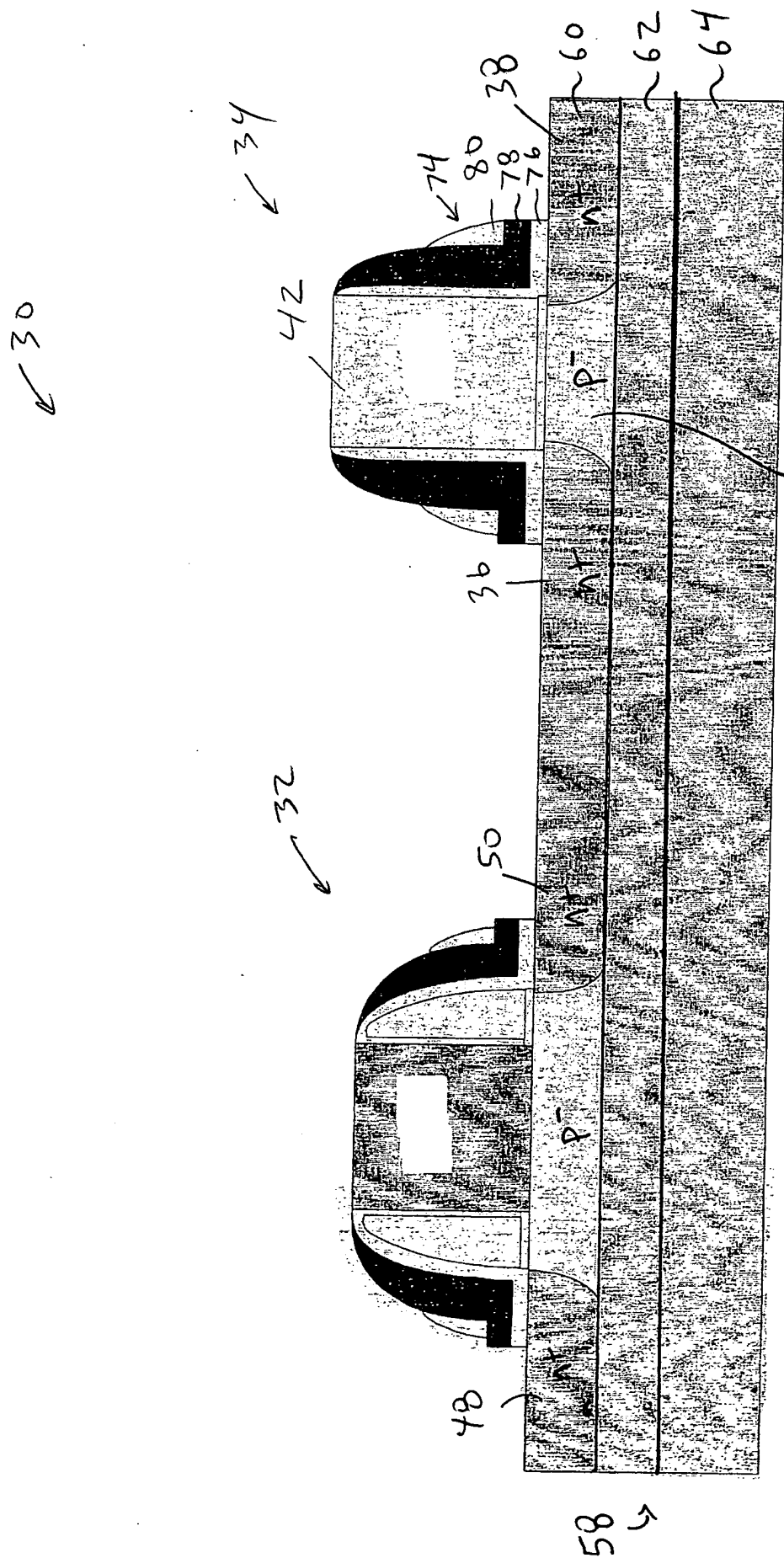


FIG. 9

30

34

44

74

32

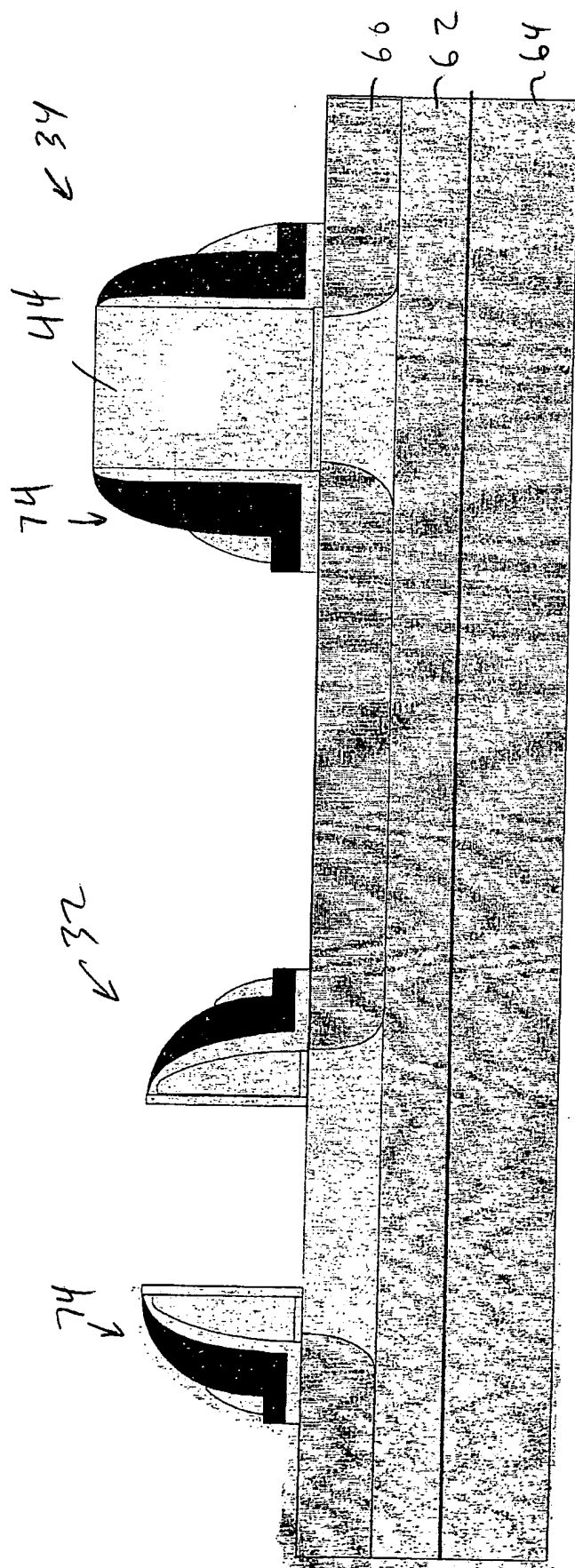
hl

66

62

64

FIG. 10



30

32

34

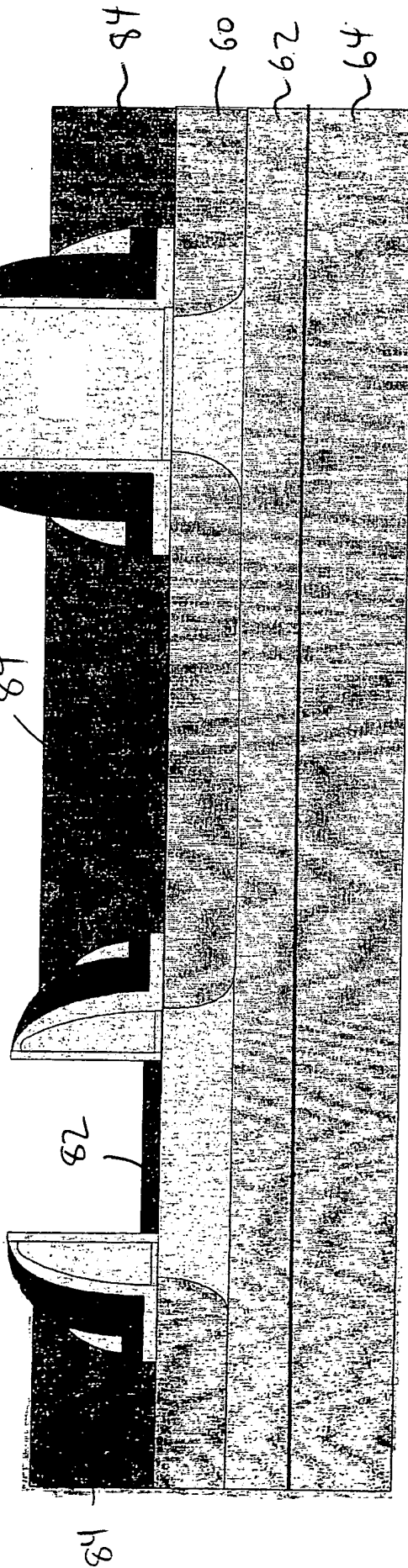


FIG. 11

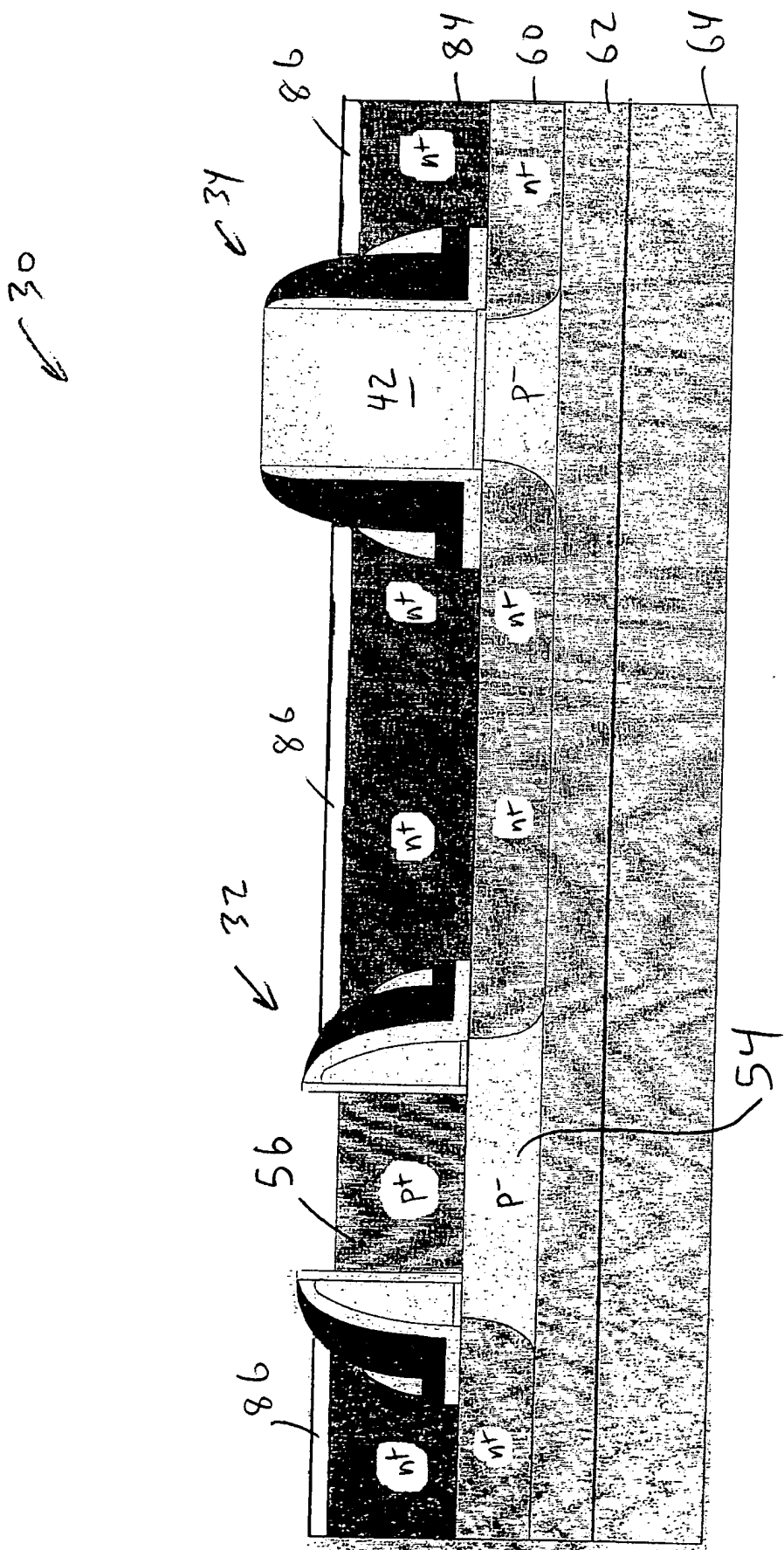


FIG. 12

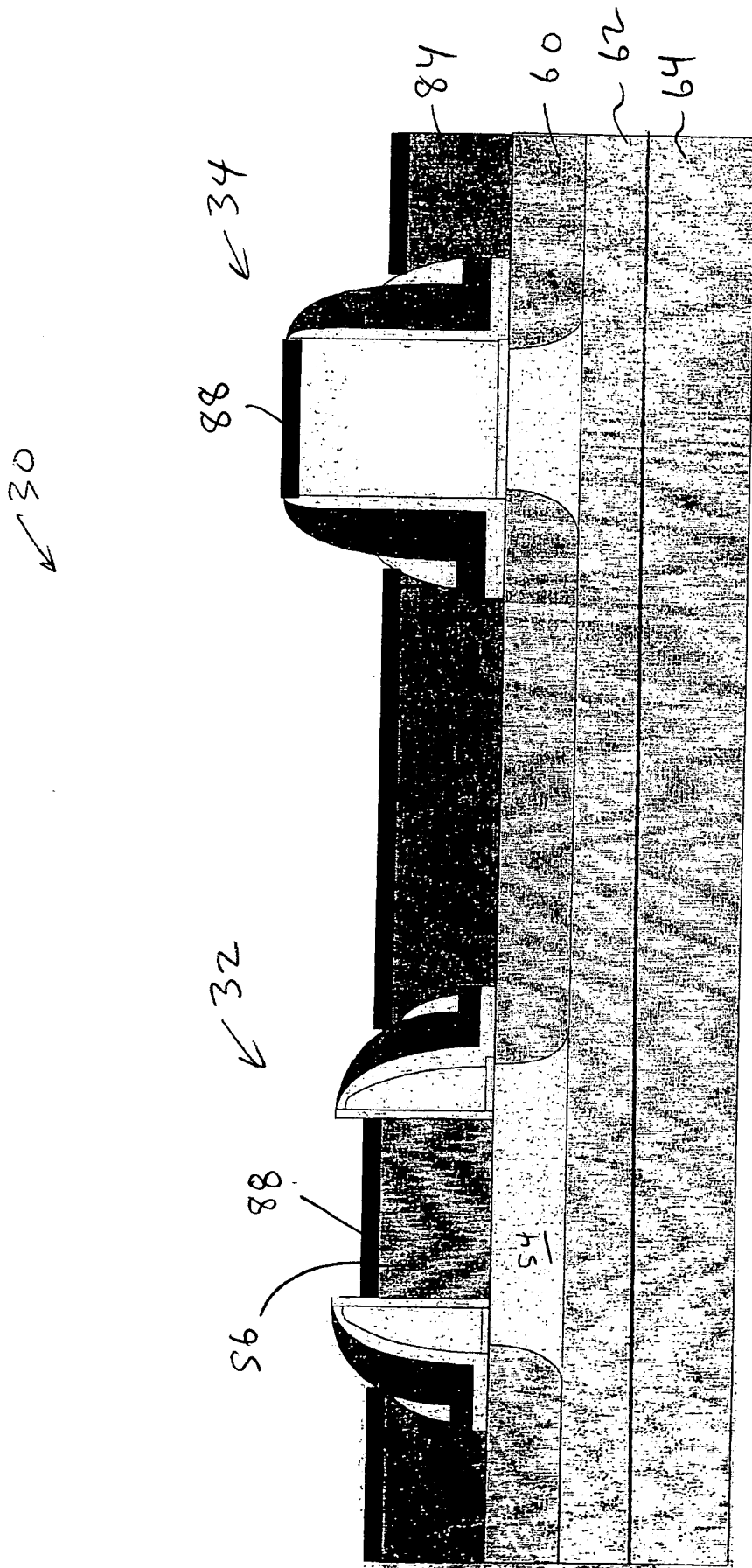


FIG. 13

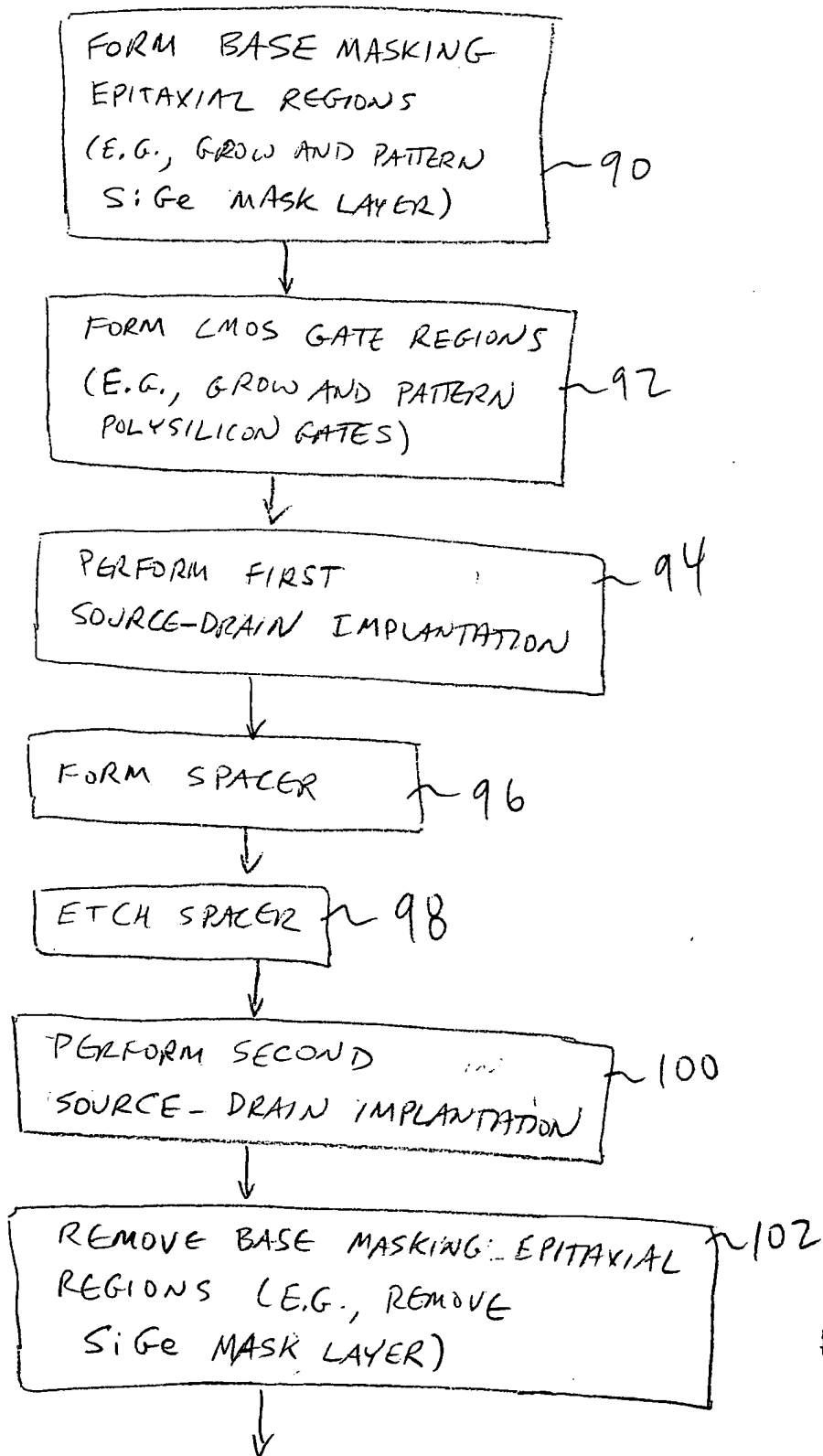


FIG. 14a

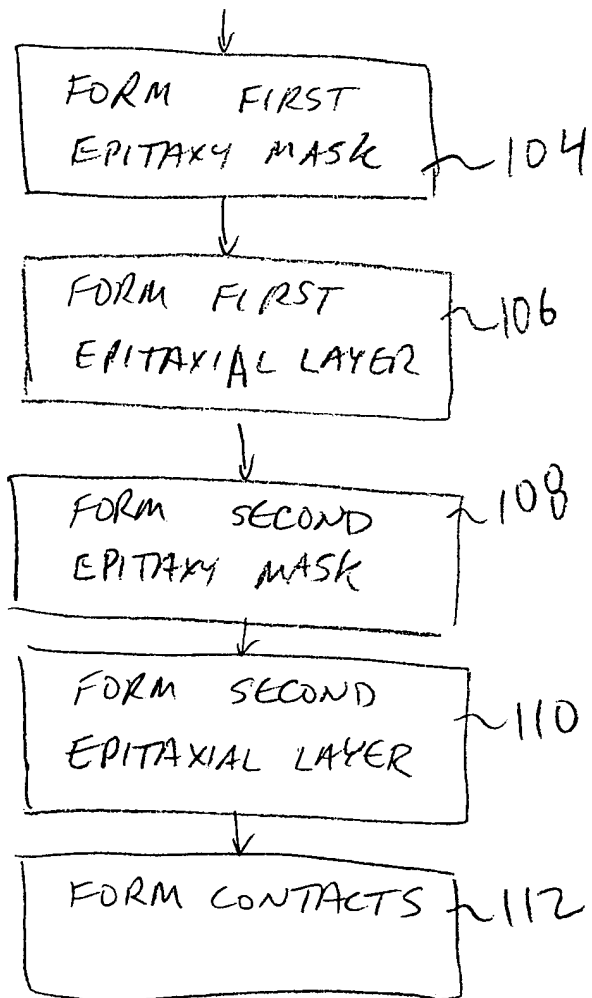


FIG. 14b

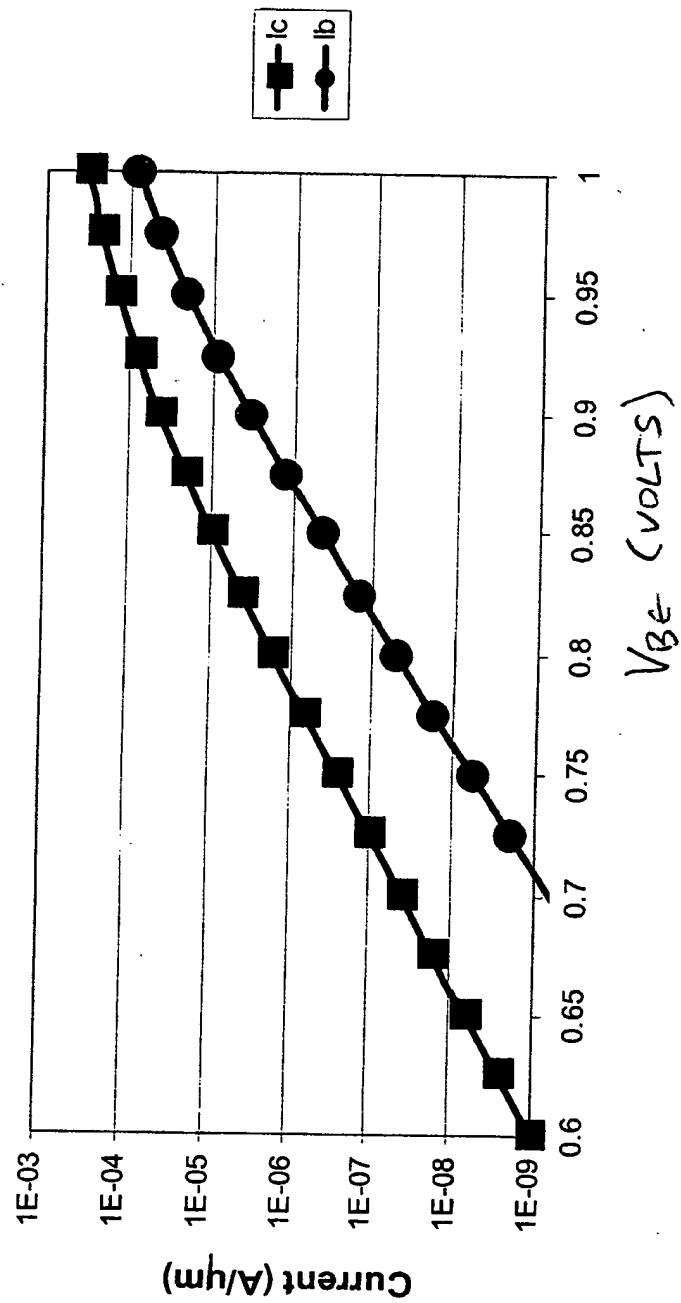


FIG. 15